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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/164,216
Filing Date	September 30, 1998
First Named Inventor	Ronald Pasqualini
Group Art Unit	2811
Examiner Name	Nadav, Ori
Total Number of Pages in This Submission: 27	Attorney Docket Number: 100-11504 (P03921-C4)

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form (in duplicate)
  - ☒ Fee Attached ($500)
- ☐ Amendment/Response
  - ☐ After Final (Response)
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☒ Appeal Brief
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Inquiry
- ☒ Other Enclosure(s) *(please identify below)*:
  Return Receipt Postcard
  Express Mail No. EV530655969US

Remarks: **Please charge any necessary fees or credit overpayment to Deposit Account No. 502305. A duplicate copy of this transmittal is attached for this purpose.**

Triplicate Copies of the Appeal Brief not included in accordance with 37 CFR §41.37(a)(1)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Mark C. Pickering, Reg. No. 36,239
Signature	Mark C. Pickering
Date	January 18, 2005

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage Express Mail No. EV530655969US in an envelope addressed to: Mail Stop Appeal Brief-Patent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date: January 18, 2005

Typed or printed name	Robin L. King		
Signature	Robin L. King	Date	January 18, 2005

FEE TRANSMITTAL
For FY 2005

Patent Fees are subject to annual revision.

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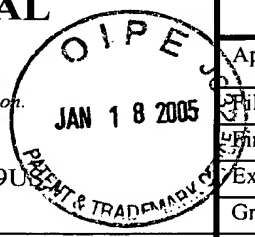

TOTAL AMOUNT OF PAYMENT	$500

Complete if Known	
Application Number	09/164,216
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Examiner Name	Nadav, Ori
Group Art Unit	2811
Attorney Document No.	100-11504 (P03921-C4)

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge any fees or credit any overpayment under 37 CFR 1.16 and 1.17 which may be required by this paper to Deposit Account No. **502305**
LAW OFFICES OF MARK C. PICKERING

☐ Applicant claims small entity status. See 37 CFR 1.27.

2. ☒ **Payment Enclosed:**
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE/SEARCH FEE/EXAMINATION FEE

LARGE ENTITY Fee Code	Fee ($)	SMALL ENTITY Fee Code	Fee ($)	Fee Description	Fee Paid
1011/1111/1311	1000	2011/2111/2311	500	Utility	
1012/1112/1312	430	2012/2112/2312	215	Design	
1013/1113/1313	660	2013/2113/2313	330	Plant	
1014/1114/1314	1400	2014/2114/2314	700	Reissue	
1005	200	2005	100	Provisional	
				SUBTOTAL (1)	0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims	Fee from below	Fee Paid
Total Claims	* - 20 **	= 0	x 50	= $ 0
Independent	* - 3	= 0	x 200	= $ 0
Multiple Dep.			*	= $ 0

** *or number previously paid, if greater; for Reissues, see below:*

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description
1202	50	2202	25	Claim in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue ind. claims over original patent
1205	50	2205	25	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)	$0

FEE CALCULATION (continued)

3. Additional Fees

Large Entity Fee Code	Fee	Small Entity Fee Code	Fee		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for ex parte reexamination	
1804	920	1804	920	Requesting publication of SIR prior to Examiner action	
1805	1840	1805	1840	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1020	2253	510	Extension for reply within third month	
1254	1590	2254	795	Extension for reply within fourth month	
1255	2160	2255	1080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500
1403	1000	2403	500	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	500	2452	250	Petition to revive-unavoidable	
1453	1500	2453	750	Petition to revive-unintentional	
1501	1400	2501	700	Utility issue fee (or reissue)	
1502	800	2502	400	Design issue fee	
1503	1100	2503	550	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention be examined (37 CFR 1.129(b)	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
*Reduced by Basic Filing Fee Paid				**SUBTOTAL (3)**	$500

SUBMITTED BY

Law Offices of Mark C. Pickering
P.O. Box 300
Petaluma, CA 94953-0300
Telephone: (707) 762-5583
Facsimile: (707) 762-5504
Customer No. 33402

Date: 1-18-05

By: Mark C. Pickering

Mark C. Pickering, Reg. No. 36,239

Express Mail Number EV530655969US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Ronald Pasqualini Appln. No.: 09/164,216 Filed: September 30, 1998 For: ESD PROTECTION CIRCUIT UTILIZING FLOATING LATERAL CLAMP DIODES	Group Art Unit: 2811 Examiner: O. Nadav APPEAL BRIEF

INTRODUCTORY COMMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an appeal from the decision dated September 1, 2004 of the Examiner finally rejecting claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72.

Real Party in Interest

The real party in interest is National Semiconductor Corporation as indicated in the assignment recorded at reel 9496, frame 0725-0726, September 30, 1998.

Related Appeals and Interferences

Appellant is not aware of any other related appeals or interferences.

Status of Claims

Claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) considered alone, or in view of the Admitted Prior Art (APA).

Claims 40-44, 58-59, 63-64, and 67-68 have been allowed.

Claims 1-14, 16-18, and 20-37 have been cancelled.

Claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72 are being appealed.

Status of Amendments

The last amendment entered into the case was Appellant's amendment filed on June 14, 2004.

Summary of Claimed Subject Matter

The subject matter of independent claim 15 is shown in appellant's FIG. 16, and is a semiconductor chip. The semiconductor chip of the present invention includes a plurality of pads (which can be read to be the elements labeled PAD as well as the pads 1620 shown in FIG. 16 and discussed on page 34, line 1 of appellant's specification). The semiconductor chip also includes an electrostatic discharge (ESD) negative ring (which can be read to be ESD negative ring 1610 shown in FIG. 16 and discussed on page 33, line 27).

In addition, the semiconductor chip includes a plurality of ESD positive lines (which can be read to be the positive ESD wires 1640-1647 shown in FIG. 16 and discussed on page 34, line 12). Further, the semiconductor chip includes a plurality of ESD switches that are connected to the positive lines and the ESD negative ring (which can be read to be the ESD switches 1625 shown in FIG. 16 and discussed on page 34, lines 1-2).

As shown in appellant's FIG. 16, the plurality of positive lines (positive ESD wires 1640-1647) are not electrically connected to each other (see also page 34, lines 14-15). Further, the plurality of positive lines (positive ESD wires 1640-1647) are not directly connected to a pad (PAD). In addition, each ESD switch (1625) is connected to a positive line (1640-1647) and the ESD negative ring (ring 1610).

The semiconductor chip further includes a plurality of first diodes (which can be read to be the lower ESD diodes 1630 shown in appellant's FIG. 16 and discussed on page 34, line 7 of appellant's specification). The first diodes (1630) are connected to the pads (PADS) so that each diode (1630) is connected to a pad (PAD) and the negative ring (1610).

The semiconductor chip further includes a plurality of second diodes (which can be read to be the upper ESD diodes 1635 shown in FIG. 16 and discussed on page 34, lines 7-8). The second diodes (1635) are connected to the pads (PADS) so that each second diode (1635) is connected to a pad (PAD) and a positive line (1640-1647).

The subject matter of independent claim 51 is shown in appellant's FIG. 16, and is a semiconductor chip. The semiconductor chip of claim 51 is the same as the semiconductor chip of claim 15 except that claim 51 drops the recitation that none of the positive lines are directly connected to a pad. In addition, claim 51 recites that a switch (1625) of the plurality of ESD switches (1625) passes a current from a positive line (1640-1647) to the negative ring (1610) when a voltage on the positive line (1640-1647) rises at a first rate (such as the rate of an ESD event).

The subject matter of independent claim 57 is shown in appellant's FIG. 16, and is a semiconductor chip. The semiconductor chip of claim 57 is the same as the semiconductor chip of claim 15 except that claim 57 recites that each first diode (1630) is connected between a pad (PAD) and the negative ring (1610), whereas claim 15 recites that each first diode (1630) is connected to a pad (PAD) and the

negative ring (1610). A first diode (1630) shown in appellant's FIG. 16 is both connected between and to a pad (PAD) and the negative ring (1610).

Claim 57 also recites that each second diode (1635) is connected between a pad (PAD) and a positive line (1640-1647), whereas claim 15 recites that each second diode (1635) is connected to a pad (PAD) and a positive line (1640-1647). A second diode (1635) shown in appellant's FIG. 16 is both connected between and to a pad PAD and a positive line (1640-1647).

The subject matter of independent claim 62 is shown in appellant's FIG. 16, and is a semiconductor chip. The semiconductor chip of claim 62 is the same as the semiconductor chip of claim 51 except that claim 62 recites that a first rate (such as an ESD rate) is faster than a second rate (such as a start up rate, see page 31, lines 23-26 and page 35, lines 1-3 of appellant's specification).

Claim 62 also recites that each first diode (1630) is connected between a pad (PAD) and the negative ring (1610), whereas claim 51 recites that each first diode (1630) is connected to a pad (PAD) and the negative ring (1610). A first diode (1630) shown in appellant's FIG. 16 is both connected between and to a pad (PAD) and the negative ring (1610).

Claim 62 also recites that each second diode (1635) is connected between a pad (PAD) and a positive line (1640-1647), whereas claim 51 recites that each second diode (1635) is connected to a pad (PAD) and a positive line (1640-1647). A second diode (1635) shown in appellant's FIG. 16 is both connected between and to a pad (PAD) and a positive line (1640-1647).

The subject matter of dependent claim 45 is shown in appellant's FIG. 16, which requires that the plurality of ESD positive lines (1640-1647) not be directly connected to a steady voltage source. As shown in FIG. 16, the plurality of ESD positive lines (1640-1647) are separated from a steady voltage source by diodes 1630 and 1635.

Grounds of Rejection to be Reviewed on Appeal

Claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) considered alone, or in view of the Admitted Prior Art (APA).

Argument

Rejection under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) considered alone, or in view of the Admitted Prior Art (APA).

Claims 15, 19, 38-39, 45-50, 57, 60-61, and 69-70

The following comments apply to claims 15, 19, 38-39, 45-50, 57, 60-61, and 69-70.

Claim 15 recites, in part,

> "a plurality of pads; [and]
> "a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad. [Brackets added.]

Independent claim 57 recites similar limitations.

In rejecting the claims, the Examiner pointed to pads P1 and P2 shown in FIG. 3 of Gens as constituting the plurality of pads. In addition, the Examiner pointed to the "horizontal lines" which are connected to the right side of the high power supply boxes labeled VDD1 and VDD2 (and the vertical extensions connected to the horizontal lines) as constituting the plurality of positive lines in Gen's structure.

The Gens reference, however, expressly teaches that the boxes P1, P2, VDD1, VDD2, VSS1, and VSS2 are pads. Boxes P1 and P2 are I/O pads, boxes VDD1 and VDD2 are power supply pads, and boxes VSS1 and VSS2 are ground pads. (See FIGS. 2 and 3, column 3, line 38, column 3, lines 44-45, and column 4, lines 5-7 of the Gens reference.) Since the horizontal lines shown in FIGS. 2 and 3 of Gens are directly connected to pads VDD1 and VDD2, it is not possible for the horizontal lines to be read to be the positive lines required by claims 15 and 57.

In responding to appellant's argument, the Examiner appears to argue that the claim term "pads" means "pads that carry varying voltages when operating normally under non-ESD conditions." In other words, the Examiner appears to argue that the claim term "pad" can not be read to be a pad that is connected to a steady voltage, such as a power supply voltage or ground, when operating normally under non-ESD conditions.

To reach this interpretation, the Examiner argues that when determining the meaning of a claim term, the Examiner may turn to the specification for assistance. In this case, because the claims were restricted to the embodiment shown in FIG. 16 (see election of species requirement dated March 23, 2000 and appellant's response dated April 13, 2000), the Examiner appears to argue that the Examiner may not consider any other portion of appellant's specification other than paragraphs which directly relate to FIG. 16.

Having focused solely on the paragraphs that directly relate to FIG. 16, the Examiner argued that appellant's specification only describes I/O pads 1620, and does not recite VCC pads and ground pads. The Examiner then concluded that because the paragraphs in appellant's specification which deal directly with FIG. 16 only describe I/O pads, then the claim term "pad" must be read to mean an "I/O pad" or a "pad that carries varying voltages when operating normally under non-ESD conditions."

Given this interpretation, the Examiner appears to argue that a pad that is connected to a steady voltage, such as a power supply voltage or ground, during non-ESD conditions can not be read to be an I/O pad. Thus, the Examiner argues that since the VDD1 and VDD2 power pads shown in FIG. 3 of Gens are connected to a steady voltage during non-ESD conditions, the VDD1 and VDD2 power pads can not be read to be pads.

Thus, the first issue addressed by the Examiner is whether the Examiner may consider other portions of appellant's specification, or whether the Examiner must limit the review to only those paragraphs that directly relate to FIG. 16 because the claims were restricted to the embodiment shown in FIG. 16. From what appellant can determine, the Examiner has not cited any authority for the argument that the Examiner must limit the review.

In the amendment filed on October 27, 2003, appellant noted that to determine the meaning of a claim term, the PTO must review the entire patent disclosure. Rowe v. Dror, 112 F.3d 473, (Fed. Cir. 1997). In view of Rowe, the Examiner must consider appellant's entire disclosure, including FIGs. 1-16, when interpreting a claim term. As a result, the Examiner erred by limiting the Examiner's review to only FIG. 16 and the associated text of appellant's specification.

From what appellant can determine, the Examiner has not addressed appellant's argument that, in view of Rowe, the Examiner must review the entire specification when interpreting the meaning of a claim term. (In the Official Action mailed September 1, 2004, the Examiner attempted to make a distinction between being connected to a pad versus being connected to said pads, which appellant respectfully does not understand.)

When considering the entire specification, appellant's specification makes numerous references to I/O pads, VCC pads, and ground pads. For example, appellant's FIG. 4 shows an I/O pad, a dirty ground pad, a substrate ground pad, a

clean ground pad, and an analog ground pad, while appellant's FIG. 6 shows an I/O pad, a dirty VCC pad, a clean VCC pad, and an analog VCC pad, and appellant's FIG. 7 shows a shared VCC pad. Thus, appellant's disclosure refers to I/O pads, VCC pads, and ground pads. Further, appellant's FIG. 16 shows numerous pads which are only labeled as pads PADS.

After the entire disclosure has been reviewed, the PTO must give the claims their broadest reasonable interpretation in light of the specification. In re Zletz, 893 F.2d 319, (Fed. Cir. 1989). Thus, since the claims require "a plurality of pads," and appellant's specification discloses I/O pads, VCC pads, and ground pads, the broadest reasonable interpretation of the claim term "pads" must include I/O pads, power pads, and ground pads.

Therefore, as required by Zletz, the claim term "pads" can not be given an interpretation that is narrower and, as a result, can not be interpreted to mean "pads that carry varying voltages when operating normally under non-ESD conditions." Thus, when the claim term "pads" is applied to the Gens reference, the claim term "pads" includes both structures that carry varying voltages and structures that carry steady voltages under non-ESD conditions. As a result, the horizontal lines shown in FIG. 3 of Gens can not be read to be the positive lines of the claims because these lines are connected to pads.

The type of input received by the pad is not claimed, and may not be read into the claim as a limitation. As a result, as noted above, the VDD1 and VDD2 power pads shown in FIG. 3 of Gens must be read to be pads. Thus, the horizontal line connected to the VDD1 and VDD2 power pads can not be read to be the positive lines required by the claims.

The Examiner also argued that it would be obvious to utilize a pair of parallel head-to-toe diodes between the power supply pad VDD1 and bus R1, citing column 4, lines 28-36 of Gens. However, using two diodes in parallel does not change the

above argument. With a pair of parallel diodes, the inputs of both diodes would be connected to the high voltage pad VDD1 via a horizontal line, which the Examiner has read to be a positive line of the plurality of positive lines. Thus, since the horizontal line that lies between power supply pad VDD1 and a pair of parallel diodes directly contacts the power supply pad VDD1, the horizontal line can not be read to be a positive line.

In response to the argument that the horizontal line identified by the Examiner can not be read to be a positive line, the Examiner appears to alternately argue, with no apparent support from Gens, that it would be obvious to place an additional diode between the power pads and the horizontal lines because such an arrangement would provide additional isolation.

For example, the Examiner appears to argue that it would be obvious to add a diode next to each power pad such that a first end contacts a pad, like power pad VDD1, and a second end contacts the horizontal line which, in turn, is connected to the diodes, like diodes D1and D2. With the addition of a diode, the Examiner argues that the horizontal lines would no longer be in direct contact with the power supply pads. The Examiner further argues that one skilled in the art would be motivated to add this additional diode to each power pad to increase isolation.

The ESD path is used to protect the gate oxide junctions of the transistors that are connected to an input node from destructive breakdown and must, therefore, be a very low impedance path. However, adding a diode adjacent to each power pad adds the impedance of two additional diodes in the ESD path, when the path begins at one power pad and ends at another power pad.

One skilled in the art would not be motivated to increase the impedance of an impedance sensitive path without some evidence that the increase in impedance provides a significant benefit. The Examiner, however, has not provided any evidence that isolation, the argued benefit, is an issue. One skilled in the art would

not be motivated to increase the impedance of an impedance sensitive path to increase the isolation if the existing isolation is fine.

In addition, the Examiner has not provided any evidence that adding additional diodes adjacent to the power pads would substantially increase the isolation. One skilled in the art would not be motivated to increase the impedance of an impedance sensitive path to increase the isolation if the resulting increase in isolation would be relatively minor.

MPEP §2142 requires the Examiner to factually support any prima facia conclusion of obviousness. In addition, if the Examiner does not produce a prima facia case, the applicant is under no obligation to submit evidence of nonobviousness. In the present case, the Examiner has not factually supported a prima facia conclusion of obviousness. The Examiner provided no evidence that isolation is an issue, or that adding diodes would substantially increase isolation.

The addition of diodes to the FIG. 3 circuit of Gens as suggested by the Examiner would significantly increase the impedance of an impedance sensitive path, going from three devices (diodes D1 and D2 and switch Z in FIG. 2) to five devices (with the addition of two diodes in a first power pad to a second power pad ESD path). As a result, one skilled in the art would not be motivated to take this step without evidence that isolation is an issue, and that adding diodes would substantially increase the isolation. Since the Examiner has not provided this evidence, the Examiner has not established a prima facia case of obviousness.

Thus, since FIG. 3 of Gens teaches that the horizontal lines identified by the Examiner as positive lines are directly connected to pads, the use of parallel diodes does not prevent a horizontal line of Gens from directly contacting a pad, and since the Examiner has not provided a prima facia case of obviousness with respect to the addition of diodes adjacent to the power pads, independent claims 15 and 57 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA).

In addition, since claims 19, 38-39, 45-50, and 69 depend either directly or indirectly on claim 15, claims 19, 38-39, 45-50, and 69 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA) for the same reasons as claim 15. Further, since 60-61 and 70 directly depend from claim 57, claims 60-61 and 70 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 57.

Claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72

The following comments apply to claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72.

Claim 15 also recites, in part,

> "an electrostatic discharge (ESD) negative ring:
> "a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;
> "a plurality of first diodes . . .; and
> a plurality of second diodes . . ..

Independent claims 51, 57, and 62 recite similar limitations.

In further rejecting the claims, the Examiner pointed to bus R2 shown in FIG. 3 of Gens as constituting the ESD negative ring, and a plurality of switches (diodes) that are connected to the ESD positive lines and the ESD negative line as constituting the ESD switches of claim 15. In addition, the Examiner pointed to diodes D2 shown in FIG. 2 of Gens as constituting the first diodes of the claims, and diodes D1 shown in FIG. 2 of Gens as constituting the second diodes of the claims.

With respect to the plurality of ESD switches, the Examiner appears to argue that the diodes D2 shown in FIG. 2 of Gens can be read to be the plurality of switches required by the claims because the diodes D2, which the Examiner has also

read to be the plurality of first diodes of the claims, are the only elements connected to both the horizontal lines (read by the Examiner to be the positive lines) and the ESD negative ring R2.

The Examiner appears to indicate that Gens does not teach that the diodes D2 shown in FIG. 2 are switches (see page 2 of September 1, 2004 Official Action, last two lines), but argues that the diodes D2 can be read to be switches because the diodes D2 are inherently switches. An ESD switch is commonly understood to be a device that remains open and prevents a current from flowing from a positive line to a negative line when a first voltage spike occurs, such as at power up, and closes and allows a current to flow from the positive line to the negative line when a second voltage spike, such as an ESD event, occurs.

The diodes D2 shown in FIG. 2 of Gens, however, never operate in this manner. When operating normally, diode D2 remains open and prevents a current from flowing from power pad VDD1 to the ESD negative ring R2. However, from what appellant can determine, there is never a normal operating instance where the diodes D2 shown in FIG. 2 of Gens close and provide a current path from power pad VDD1 to the ESD negative ring R2. Thus, since the diodes D2 are never operated as switches, these devices can not be read to be switches.

In the alternative, the Examiner argues that appellant's FIG. 1 and FIG. 2 (the APA) show a plurality of ESD switches connected to the positive line and the negative ring. Appellant notes, however, that appellant's FIG. 1A, FIG. 1B, and FIG. 2 each show only one switch, switch 130 shown in FIGS. 1A and 1B, and switch 210 in FIG. 2. Thus, each figure of the APA shows only a single ESD switch.

The Examiner further argued that it would also have been obvious to connect a plurality of switches between the horizontal (positive) lines and the ESD negative ring R2 in Gens in order to provide a more effective uni-directional flow of current during ESD operation. Since the Examiner has read the horizontal lines connected to

the power supply pad VDD1 to be the positive lines, the Examiner has effectively argued that it would be obvious to connect a switch between the power supply pad VDD1 and the ESD negative ring R2 of Gens in order to provide a more effective uni-directional flow of current during ESD operation.

The Examiner, however, has not provided any evidence that adding switches to Gens in this manner would improve the current flow during an ESD event, or even allow the Gens circuit to operate as intended. (If an added switch between the power supply pad VDD1 and bus R2 breaks down and provides current path to bus R2 before switch Z shown in Gens FIG. 2, the FIG. 2 circuit of Gens will not operate as intended. If the added switch breaks down after switch Z, then the added switch provides no benefit.)

As a result, the Examiner has not established a prima facia case of obviousness. Thus, since the diodes D2 shown in FIG. 2 of Gens never function as a switch between a power pad and bus R2, and the Examiner did not set forth a prima facia case of obviousness with regard to adding switches to Gens, independent claims 15, 51, 57, and 62 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA).

In addition, since claims 19, 38-39, 45-50, and 69 depend either directly or indirectly on claim 15, claims 19, 38-39, 45-50, and 69 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA) for the same reasons as claim 15. Further, since claims 52-56 and 71 directly depend from claim 51, claims 52-56 and 71 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 51. Since claims 60-61 and 70 directly depend from claim 57, claims 60-61 and 70 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 57. Since claims 65-66 and 72 directly depend from claim 62, claims 65-66 and 72 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 62.

Claims 45-47

The following comments apply to claims 45-47.

In rejecting claim 45, the Examiner stated that Gens teaches a plurality of ESD positive lines that are not directly connected to a steady voltage source. The Examiner, however, has pointed to the horizontal lines connected to the power pads, e.g., VDD1 and VDD2, as constituting the plurality of ESD positive lines required by the claims. If the horizontal lines identified by the Examiner are read to be the positive lines required by the claims, then the Gens reference teaches that these horizontal lines are directly connected to the power pads VDD1 and VDD2, which are steady voltage sources when operating normally. Thus, claim 45 is patentable over Gens, and Gens in view of the Admitted Prior Art (APA) for these additional reasons. Furher, since claims 46 and 47 directly and indirectly depend from claim 45, claims 46 and 47 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 45.

Claims 51-56, 71, 62, 65-66, and 72

The following comments apply to claims 51-56, 71, 62, 65-66, and 72.

Independent claims 51 and 62 also require that a switch pass a current from a positive line to the negative ring. The Examiner pointed to FIG. 2 of appellant's specification (the APA) as teaching an ESD switch that includes a transistor. (The ESD switch shown in APA FIG. 2 uses three transistors.) The Examiner argued that the APA ESD switch passes current when a voltage rises at a first rate.

The Examiner next appears to argue that it would be obvious to use the ESD transistors shown in FIG. 2 of the APA between each horizontal line (which has been

read to be a positive line), and the bus R2. Since each horizontal line is directly connected to a power pad, the Examiner is effectively arguing that it would be obvious to use the ESD transistors shown in FIG. 2 of the APA between each power pad, e.g., pads VDD1 and VDD2, and the bus R2.

The Examiner argued that one skilled in the art would be motivated to add the ESD transistors in order to improve the switching capabilities of the device during an ESD event. However, adding the ESD transistors to each power pad would increase the area consumed by the ESD protection circuit. One skilled in the art would not be motivated to add devices and consume circuit area without some evidence that the use of the ESD transistors would improve switching.

The Examiner, however, has not provided any evidence that adding the APA ESD transistors shown in FIG. 2 in this way would improve the switching capabilities, or even allow the Gens circuits to operate as intended. As a result, the Examiner has not established a prima facia case of obviousness. Thus, claims independent claims 51 and 62 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA) for these additional reasons. Further, since claims 52-56 and 71 directly depend from claim 51, claims 52-56 and 71 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 51. Further, since claims 65-66 and 72 directly depend from claim 62, claims 65-66 and 72 are patentable over Gens, and Gens in view of the APA for the same reasons as claim 62.

Conclusion

The Examiner's rejections are clearly erroneous and should be reversed.

Respectfully submitted,

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Mark C. Pickering
Registration No. 36,239
Attorney for Applicant

30 Fifth Street, Suite 200
P.O. Box 300
Petaluma, CA 94953-0300
Telephone: (707) 762-5500
Facsimile: (707) 762-5504
Customer No. 33402

CLAIMS APPENDIX

15. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

19. The chip of claim 15 wherein the ESD negative ring encircles the periphery of the chip.

38. The chip of claim 19 wherein none of the plurality of positive lines encircles the periphery of the chip.

39. The chip of claim 15 wherein a switch of the plurality of switches includes a transistor connected to a positive line and the negative ring.

45. The chip of claim 15 wherein the ESD positive lines are never directly connected to a steady voltage source.

46. The chip of claim 45 wherein each second diode has an anode electrically connected to a pad.

47. The chip of claim 46 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

48. The chip of claim 15 wherein each second diode has an anode electrically connected to a pad.

49. The chip of claim 48 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

50. The chip of claim 15 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

51. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a

positive line to the negative ring when a voltage on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

52. The chip of claim 51 wherein the switch blocks a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

53. The chip of claim 51 wherein a second diode is forward biased when the voltage on the positive line rises at the second rate.

54. The chip of claim 51 wherein none of the plurality of positive lines encircles the periphery of the chip.

55. The chip of claim 51 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

56. The chip of claim 51 wherein an ESD switch is directly connected to a positive line and the negative ring.

57. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

60. The semiconductor chip of claim 57 wherein an ESD switch is directly connected to a positive line and the negative ring.

61. The semiconductor chip of claim 57 wherein none of the positive lines encircles the periphery of the chip.

62. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a

positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

65. The semiconductor chip of claim 62 wherein an ESD switch is directly connected to a positive line and the negative ring.

66. The semiconductor chip of claim 62 wherein none of the positive lines encircles the periphery of the chip.

69. The chip of claim 15 wherein a second diode is directly connected to a pad and directly connected to a positive line.

70. The chip of claim 57 wherein a second diode is directly connected to a pad and directly connected to a positive line.

71. The chip of claim 51 wherein a second diode is directly connected to a pad and directly connected to a positive line.

72. The chip of claim 62 wherein a second diode is directly connected to a pad and directly connected to a positive line.

EVIDENCE APPENDIX

The Evidence Appendix is empty.

RELATED PROCEEDINGS APPENDIX

The Related Proceedings Appendix is empty.